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Interface Sheet-IS

IS-47-41-005 Interface Sheet between PBS47 (PCS) and PBS 41 (CPSS – VS3) – Architecture

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Approval Process			
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Change Log			
IS-47-41-005 Interface Sheet between PBS47 (PCS) and PBS 41 (CPSS – VS3) – Architecture (7PE9R4)			
Version	***Latest Status***	***Issue Date***	***Description of Change***
v0.0	In Work	21 Apr 2022	
v1.0	In Work	08 Dec 2023	Major update of requirements
v1.1	Revision Required	16 Oct 2025	First issue for review. Details on distribution of operating cycles will be included in next revision.
v1.2	Approved	16 Dec 2025	Minor revision including: - incorporation of reviewer comments - textual improvements - clarification of unused coil termination responsibilities - removal of crowbar service life requirement - update of Figure 6.2 for clarity - update of applicable & reference document versions The distribution of plasma pulse types (Table 7-2) is to be defined in a future version once the data is available. The document with tracked changes is included as attachment.

Table of Contents

1 Purpose

The purpose of this Interface Sheet (IS) is to define the interface requirements associated to the interfaces between the Plasma Control System (PBS 47) and the VS3 Power Supply (PBS 41) in agreement with ICD-47-41 [AD 1].

This IS-47-41-005 is focused on the functional relation between the PCS and the VS3 Power Supply to allow the PCS performing the required plasma controls activities. It will not cover the technical details of the implementation (hardware and software) of the interface nor the physical interface between the two systems in the scope of PBS-45 CODAC.

The present version is developed in the framework of the VS3-PS Conceptual Design stage. Although many detailed values are stated in this version, they are included for the sake of completeness of the interface definition and are subject to change following the preliminary and final design stages.

2 Acronyms & Definitions

2.1 Acronyms

AC	Alternating Current
CDR	Conceptual Design Review
CIS	Central Interlock System
dBFS	decibels relative to Full Scale
DC	Direct Current
DR	Dynamic Range
DT-1	First Deuterium-Tritium phase
DT-2	Second Deuterium-Tritium phase
ESCB	Energy Storage Capacitor Bank
FDR	Final Design Review
FOCS	Fiber-Optic Current Sensor
FSR	Full Scale Range
ICD	Interface Control Document
IP	Interface Point
IR	Interface Requirement
IS	Interface Sheet
NA	Not Applicable
OCL	Over-Current Limiting
OCP	Over-Current Protection
OCT	Over-Current Tripping
OVL	Over-Voltage Limiting

OVP	Over-Voltage Protection
OVT	Over-Voltage Tripping
PA	Procurement Arrangement
PCS	Plasma Control System
PS	Power Supply
PBS	Plant Breakdown Structure
PDR	Preliminary Design Review
RMS	Root Mean Square
SNR	Signal-to-Noise Ratio
SRD	System Requirements Document
SRO	Start of Research Operation
TBD	To Be Defined
VDE	Vertical Displacement Event
VS3	Vertical Stabilization 3
VV	Vacuum Vessel

The full list is detailed in the document: ITER Abbreviations: ITER_D_2MU6W5.

2.2 Definitions

Dynamic Range	Ratio between the largest and smallest measurable values of a specific quantity
Minor VDE	Temporary but recoverable loss of plasma vertical stabilization [RD1]. Covers the 60/80kA peak current profile used as main design input for VS3-PS.
Pulse	Any pulsed current delivered by the power supply into the VS3 coil circuit exceeding 20 kApk for any duration. Includes MinorVDE pulses.
Signal-to-Noise Ratio	Ratio of the signal power to the noise power, tyicall expressed in decibels.
Tokamak pulse	ITER Tokamak plasma operation, consisting of ramp-up, flat-top and ramp-down phases. Defined in accordance with [RD2].

3 Applicable Documents

Ref	Document Title	UID	Version
[AD1]	Interface Control Document for Plasma Control System (PBS 47) and Coil Power Supplies & Distribution (PBS 41)	ITER_D_33KFL9	4.1
[AD2]	SRD-41 (Coil Power Supply and Distribution) from DOORS	ITER_D_28B6XQ	6.0
[AD3]	SRD-47 (PCS) from DOORS	ITER_D_2M77K4	6.10
[AD4]	Plasma Control System Physics Requirements Document	ITER_D_BH2429	1.7
[AD5]	ITER Research Plan	ITER_D_YS74S9	-
[AD6]	Plant Control Design Handbook	ITER_D_27LH2V	7.1
[AD7]	Staged Approach Configuration	ITER_D_SNE6G8	4.1

4 Reference Documents

Ref	Document Title	UID	Version
[RD1]	In-vessel coil currents and fusion power scenarios for the evaluation of the in-vessel coils fatigue lifetime	ITER_D_SQFNJF	1.1
[RD2]	Project Requirements (PR)	ITER_D_27ZRW8	7.1
[RD3]	Project Requirements (PR)	ITER_D_27ZRW8	6.3
[RD4]	Functional Interface between Plasma Control and In-Vessel coils	ITER_D_P7M9N4	6.3
[RD5]	Transient Operation of VS3 System Including Inductive Coupling to Passive Structure	ITER_D_VXWY3N	1.0
[RD6]	In-Vessel Coils Detailed Design Description	ITER_D_4B9A6E	3.1
[RD7]	VS3-PS System Design Description	ITER_D_DF8QNV	1.1
[RD8]	VS3-PS Functional Analysis Report for CDR	ITER_D_DF8TZX	1.0

5 Interfaces Identification

The main purpose of the VS3 Power Supply (PS) is to generate controlled current/voltage in the VS3 coil circuit during plasma ramp-up, flat-top, and ramp-down, under the command of PCS. Additional support functions involving the VS coils and VS3-PS during e.g. commissioning and calibration activities may be anticipated within the limits defined by the requirements originating from this main purpose.

Operation of ITER requires active control of the plasma's vertical position, which in part is accomplished through the Vertical Stabilization (VS) coils that reside inside the Vacuum Vessel (VV). The VS coils consist of an upper and lower solenoidal coil, VS3U and VS3L respectively, connected in an anti-series "saddle" arrangement for all normal operating scenarios. Both upper and lower VS coil are comprised of 4 individual turns, interconnected by the VS3 Linkboard.

The plasma's vertical position is stabilized by a feedback system that typically measures the vertical drift velocity and controls the current in the VS coils to generate a horizontal magnetic field that counteracts the vertical displacement. The VS coils thus exert a downward force on the plasma when it drifts upwards, and vice versa. The control loop including power supply and coil needs to be capable of responding fast enough for both stabilization and VDE avoidance purposes.

The VS3 Power Supply performs the following functions in relation to PCS:

1. To generate controlled voltage / current in the VS coil circuit as requested by PCS for:
    a. Vertical plasma stabilization
    b. Mitigating Vertical Displacement Events (VDEs)
2. To acquire and transmit to PCS the electrical quantities relevant for control of plasma
3. To monitor and transmit to PCS the operational status and health of VS3 PS

In consideration of the above, the following interface points have been identified:

Table 5-1: Interfaces identification

IP No.	IP Title	PBS 47				PBS 41			
		Designation	**Reference**	**PIC (Y/ N)**	**Procure ment**	**Designation**	**Reference**	**PIC (Y/N)**	**Procure ment**
1	System and performance requirements	Control Functions: Support Functions / Kinetic Control	47.CF.SF / 47.CF.KC	N	IO	VS3 Power Supply	41.V3	N	IO
2	Measurements	Control Functions: Support Functions	47.CF.SF	N	IO	VS3 Power Supply	41.V3	N	IO
3	Status Reporting	Control Functions: Support Functions	47.CF.SF	N	IO	VS3 Power Supply	41.V3	N	IO

IP No.	IP Title	PBS 47				PBS 41			
		Designation	Reference	PIC (Y/N)	Procurement	Designation	Reference	PIC (Y/N)	Procurement
4	Control signals	Control Functions: Support Functions	47.CF.SF	N	IO	VS3 Power Supply	41.V3	N	IO
5	General requirements	Control Functions	47.CF	N	IO	VS3 Power Supply	41.V3	N	IO

6 Interface description

The VS3 Power Supply consists of two independent power converters, each comprising a rectifier (charger) stage, an Energy Storage Capacitor Bank (ESCB) and an inverter stage. The two power converters are connected to the two VS coils in a Push-Pull configuration: each coil's terminals are connected to both converters. The resulting architecture has several advantages including reduced voltage stress on busbars and coils and segmentation of the stored energy.

The VS3 Local Controller controls the two power converter stages to generate the voltage and current waveforms that are requested by PCS. Hence the interface with PCS is with the local controller; the deployment and operation of the two individual power converter stages is outside of PCS' control. Measurements and status reporting are nevertheless provided for each power converter separately, for the purpose of providing additional insights in the coil circuit operation.

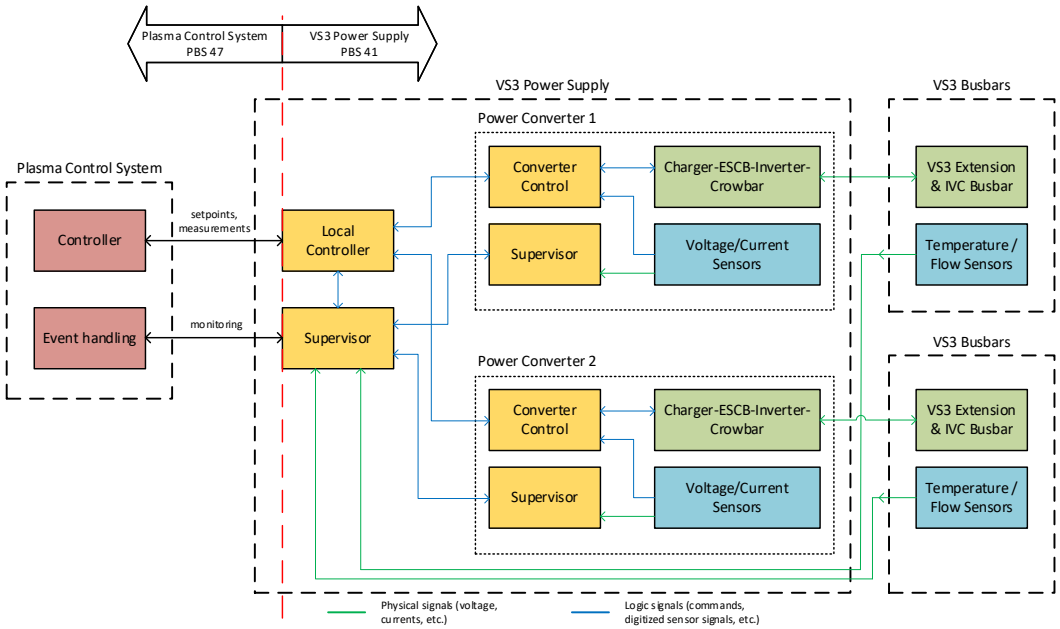

Figure 6-1: preliminary functional block diagram of the interface between PCS and VS3 Power Supply.

Monitoring of the VS3 busbar temperature and avoiding over-temperature conditions is performed by the VS3 power supply's local controller. PCS will be informed of any anomalies through the regular status flags or operational states (e.g. Fault in case of over-temperature).

The monitoring and active protection of the VS coils is accomplished through interfaces between PBS 15.IV and PCS [RD4] for avoidance and between PBS 15.IV and CIS for mitigation and protection. The VS3 Power Supply does not receive nor act on information regarding the VS coil status, but contributes to the protection by acting as actuator for CIS: it switches off and/or trigger the crowbar upon receipt of the corresponding interlock signals from CIS.

6.1 Protection mechanisms relevant to PCS

The information in the forthcoming sections is provided for awareness on the presence and operational characteristics of the VS3-PS protection mechanisms relevant to PCS, so that

unintended tripping and thereby unavailability of the power supply can be avoided. For more detailed and definitive information, the System Design Description at FDR stage or beyond is to be consulted.

The VS3-PS contains several output protection mechanisms, including but not limited to:

Protection mechanism		Scope [1]	Accessibility [2]
1.	Over-Voltage Limiting & Over-Current Limiting	Operational, Integrity	R/W
2.	Over-Voltage Tripping & Over-Current Tripping	Operational, Integrity	R/W
3.	Thermal Over-Current Protection (I^2*t)	Integrity	R
4.	Instantaneous Over-Current Protection	Integrity	-

Note 1: scope of the protection
- Operational: deployed to respect limits set for specific operating scenarios, typically user limits
- Integrity: deployed to protect the VS3-PS system integrity, typically design limits

Note 2: accessibility of the protection for operation
- R: read access, i.e. the trip/limit value and status of the protection is available for monitoring
- W: write access, i.e. the trip/limit value of the protection may be set (programmed)
- R/W: read and write access

The OVL/OCL and OVT/OCT mechanisms may be used to ensure the power supply output does not exceed pre-defined limits (which may be lower than design limits), for example during integrated commissioning activities with progressively increasing voltage/current levels.

When Protection 1 is activated, the power supply remains operational, yet with actively limited output. Protection 2 typically results in a tripped, but still operational power supply system (refer toTable 7-4). Protection 3 may result in either an actively limited output, or in a tripped power supply (TBC during FDR). Protection 4 and other built-in protections typically triggering the Fault state with the power supply transitioning to the OFF state.

In case of tripping of the power supply, the VS coils may be discharged through the crowbar (energy dissipated in coil circuit) or through the inverter stage (energy transferred to DC Link).

6.1.1 Over-Voltage Limiting (OVL) & Over-Current Limiting (OCL)

As first layer of protection, the VS3-PS will limit the output voltage and output current to the values set in respectively the Over-Voltage Limit (OVL) and Over-Current Limit (OCL) parameters. Consequently, under normal conditions, the voltage and current levels in the VS3 coil circuit will not exceed the pre-defined limits.

The status of activation, i.e. whether the output is being actively limited or not, can be monitored through the Out-of-Regulation status flag, refer to Table 7-5.

The OVL/OCL applied to the output is the most restrictive limit from the set of:

- intrinsic (design ratings) limits,
- programmed (user) limits, and
- dynamic thermal protection limits.

6.1.2 Over-Voltage Tripping (OVT) & Over-Current Tripping (OCT)

A second layer of protection is provided through OVT and OCT, which will trip the power supply operation in case any of the pre-defined limits in the respective parameters is exceeded. When tripped, the inverter output is switched off, but the DC Link remains energized (refer to Table 7-4).
This protection is always active. The programmed threshold levels for the OVT/OCT with respect to those for OVL/OCL define the priority of the tripping versus the limiting action, i.e. which protection acts first. In case of highly transient behaviour such as during faults, the priority may not always be respected: the power supply could trip before any meaningful limiting acting has been performed.
The trip limits are programmable and by default set slightly above the nominal ratings of the power supply.
The status of activation, i.e. whether or not the output has been tripped or not, is reflected in the power supply operating state, see Table 7-4.

6.1.3 Thermal Over-Current Protection (Thermal-OCP)

The VS3 Power Supply includes thermal over-current protection to ensure that the provided setpoints do not result in operation outside of the power supply (thermal) design limits. Such protection may comprise an inverse-time relay or an (I^2*t)-like protection, where the permissible RMS current level as function of time duration is set slightly above the I^2*t value of the VDE pulse.
Figure 6-2 shows the resulting duration-dependent permissible RMS current levels of the equivalent I^2*t value of the 6-turn MinorVDE pulse, including lower bound established by the continuous RMS output current rating of the power supply. For pulsed operation with pulse durations below approximately 0.5 to 1 seconds, the thermal over-current protection is still active, yet other over-current protections are likely to act before.
It is to be noted that the curve does not constitute a definition of the working area of the power supply: whether or not VS3-PS is capable of providing and sustaining a certain current level for a certain duration depends on the impedance, i.e. the required voltage, and thus power involved, as well as the integral of power in relation to the energy available in the ESCB.
The thermal OCP is focused on protection of the power supply itself, more specifically the inverter and output stage. It is not aimed (specifically) at protecting other components in the VS3 coil circuit, such as the VS coils.
The exact implementation, thresholds and the action upon triggering (i.e. tripping or limiting) is subject of the detailed design phase and will be confirmed during FDR stage.

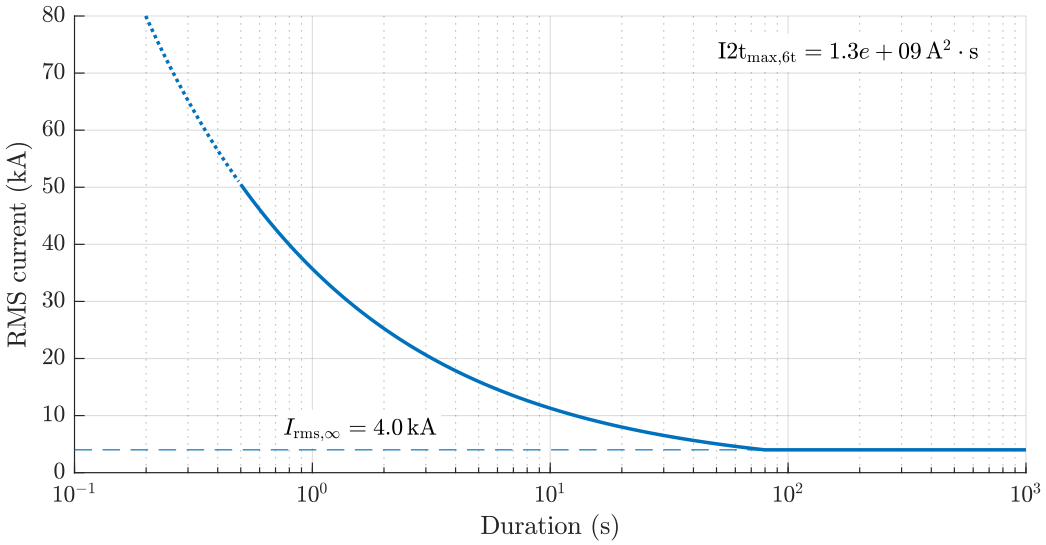

Figure 6-2: illustration of possible implementation of thermal over-current protection through I^2t-protection, showing permissible RMS current as function of the duration. The area above the curve represents the tripping area.

6.1.4 Instantaneous Over-Current Protection

Among the final layers of protection is the Instantaneous Over-Current Protection, which typically involves disabling the power converters' switching signals and triggering the crowbar upon the detection of current levels above the nominal peak current rating of the power supply, e.g. at 85 kA. The Fault state is triggered, and the power supply transitions to the OFF state. This protection is aimed at protecting the VS coils against power supply faults and the power supply against (fast) induced currents.

7 Interface Requirements (IR)

7.1 System and supplementary performance requirements

This section defines the system requirements of the VS3 Power Supply relevant to PCS. Whereas partial overlap with SRD-41 [AD2] may exist, the purpose of this section is to supplement the existing requirements where relevant for the interface between VS3 Power Supply and PCS. In case of conflict, the performance requirements set out in SRD-41 take precedence over the values stated in this IS.

[4741-005i101-R] The VS3 Power Supply shall be capable of four-quadrant operation and providing controlled voltage and current to the VS coils for fast vertical stabilization control of the plasma, with the performance requirements of Table 7-1.

> **[I]** The continuous noise RMS current is based on uniformly distributed noise in the dz/dt measurement with an RMS value of 0.6 m/s and a bandwidth of 1 kHz.

[4741-005i102-R] The VS3 Power Supply shall support two operating regimes, namely (1) providing continuous noise current for vertical stabilization control and (2) providing fast and high current pulses with a duration approximately of 0.32 seconds (including ramping up/down) in response to Minor VDEs. These operating regimes may be concurrent, yet the instantaneous current never exceeds the peak current of the VDE pulse.

> **[I]** Other operating modes, e.g. those requiring power supply duty of several (tens) of seconds, may be supported within the operating limits defined by the Noise and Minor VDE requirements. The preliminary operational limits for such intermediate duration pulses can be provided at PDR stage and confirmed at FDR stage.

Table 7-1: operational requirements for VS3-PS

	Noise (continuous)	**Minor VDE (pulsed)**
Output voltage, max. (no load)	2.4 kV	
Output current	4 kA rms – 6 turns 3 kA rms – 8 turns	80 kA pk – 6 turns 60 kA pk – 8 turns
Pulse duration	Continuous	≤ 0.32 seconds
Pulse period	-	10 s

[4741-005i103-R] The VS3 Power Supply shall be able to provide an equivalent level of performance with only 6 VS-coil turns in service, symmetrically distributed over the upper and lower coil, which means providing up to 240 kA-turn in both upper and lower VS-coil (i.e. 80 kA instead of 60 kA).

[4741-005i104-R] The VS3 Power Supply shall permit the connection and the controlled operation of the following VS coil configurations, for which the performance requirements only apply to the default anti-series connection:

1. Anti-series connection of VS3U and VS3L (symmetric number of turns)

2. Series connection of VS3U and VS3L (symmetric number of turns)
3. Single connection of either VS3U or VS3L

[I] The physical turn configuration is made manually at the VS3 Linkboard (41.V3.BB)

[I] The VS3 Linkboard facilitates the reconfiguration of VS3U / VS3L coil turns, yet the appropriate termination of unused / isolated turns is outside the scope of PBS 41.

[I] Changing from anti-series to series connection changes the power supply load impedance. Consequently, the power supply performance may be reduced.

[4741-005i105-R] The output voltage accuracy for steady-state (DC) setpoint values shall be better or equal to 1% of the rated output voltage.

[I] With the output voltage accuracy defined as the instantaneous difference between actual output voltage and the setpoint value, the output voltage accuracy for dynamic setpoints is to be expected considerably lower, due to limit control bandwidth and the overshoot resulting from the required response time.

[4741-005i106-R] The VS3 Power Supply shall be available for the entire duration of the Tokamak pulse.

[I] During any Tokamak pulse, the number of MinorVDE events to be handled by the power supply is limited to a maximum of three, after which only noise current operation may continue for the remaining of the plasma pulse.

[4741-005i107-R] The VS3 Power Supply shall be designed for the service life and pulse occurrences set out in Table 7-2. The service life requirements apply irrespective of the VS coil configuration, i.e. either 6-turn or 8-turn operation, or a combination of both over the service life of the power supply. The maximum number of Minor VDE pulses is limited to 30,000 over the total of 30,000 Tokamak pulses.

Table 7-2: service life requirements

Parameter	**Value**			**Source** [27ZRW8 v7.1]
Design life	20 years			PR1827-R
Number of Tokamak pulses	30,000			PR904-R
Tokamak pulse repetition time	≤ 1800 s for $t_{burn} \leq 450s$			PR907-R
	≤ $4*t_{burn-1}$ for $t_{burn} > 450s$ (i.e. duty cycle ≥ 25%)			
Tokamak burn time (typ.) Note 1,2	Inductive operation	450 s	(TBD) %	PR515-R
	Hybrid operation	1000 s	(TBD) %	
	Non-inductive op.	3000 s	(TBD) %	

Note 1: The entire Tokamak pulse duration comprises the following intervals:
- Ramp-up: increase of plasma current (typically 10-100s)
- Flat-top: static plasma current (comprising entry, burn, exit)
- Ramp-down: decrease of plasma current to zero (typically 3 times ramp-up time)

Note 2: Distribution of plasma pulse types as per XXX (UID to be provided)

[4741-005i108-R] PCS shall limit the number of requested Minor VDE pulses to a maximum of three per plasma pulse, and with a repetition frequency not exceeding 0.1 Hz.

[4741-005i109-R] For noise operation following a VDE pulse, PCS shall consider the limited output voltage capabilities of VS3-PS during the recharging of the ESCB from the minimum to nominal DC Link voltage.

> **[I]** The VS3-PS is not required to provide noise current requiring an output voltage exceeding the minimum DC-Link voltage (e.g. 50% of nominal voltage) while recharging after a VDE pulse. The available voltage for noise current operation is that of the (increasing) DC Link voltage.

[4741-005i110-R] The response time of the VS3 Power Supply, defined as the time between the arrival at the VS3-PS local controller of the PCS command requesting a 100% step change in output voltage and the actual rise of converter output to 90% of that voltage, shall be less than 5 milliseconds.

> **[I]** The response time comprises the delay time t_d and rise time t_r, in accordance with Figure 7-1. The delay time includes the latency in I&C electronics, networking, power converter switching cycles, etc. The rise time takes into account the dynamics of the closed-loop controller, the converter output filters, circuit parasitics, etc.
>
> **[I]** The definition of the converter output voltage location is in accordance with Figure 7-2, i.e. at the inverter output and not at the VS3 Linkboard or VS-coil terminals.
>
> **[I]** The time-constant of the VS coil is in the order of 90 ms.

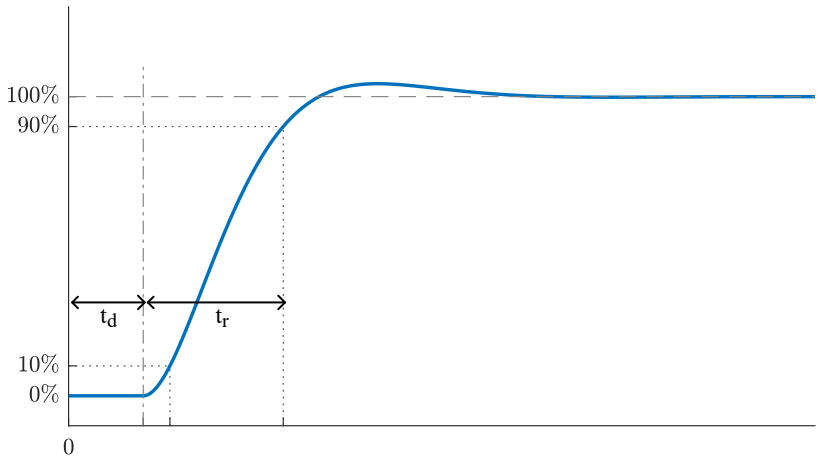

Figure 7-1: definitions for power supply response time, for a step input at time t=0

[4741-005i111-R] The VS3 Power Supply shall prevent any current from circulating in the VS3 coil circuit when the system is not required to operate during the Tokamak pulse. This requirement applies to all coil turns actively connected to the power supply through the VS3 Linkboard, and for (induced) coil circuit voltages not exceeding the nominal DC Link voltage.

[I] When the (induced) voltage in the VS3 coil circuit exceeds the nominal DC Link voltage, even when disabled, the power supply output stage may become conductive.

7.2 VS3-PS Measurements

This section defines the requirements in relation to the measurements relevant to PCS.

[4741-005i201-R] The VS3 Power Supply shall provide the following measurements to PCS:

- VS coil current
- Power supply output current(s)
- Power supply output voltage(s)
- Power supply DC link voltage(s)

[I] The VS3 Power Supply consists of two power converters in push-pull configuration. All power supply related measurements are provided for both converters. The VS coil current is provided redundantly in the form of readings of the current sensors downstream the two crowbar may be provided from a sensor downstream the crowbar of any of the two power converters.

[I] The VS coil current is measured at the output of the power supply, directly downstream of the crowbar. Consequently, leakage (non-zero conductivity) and displacement (stray capacitance) currents of the busbars/feeders dielectrics are included in the measurement.

[I] All measured voltages provided to PCS relate to differential voltages; the voltage levels with respect to earth are not provided.

[I] The VS3 Power Supply crowbar current may be derived by PCS as difference between the VS coil current and the PS output current

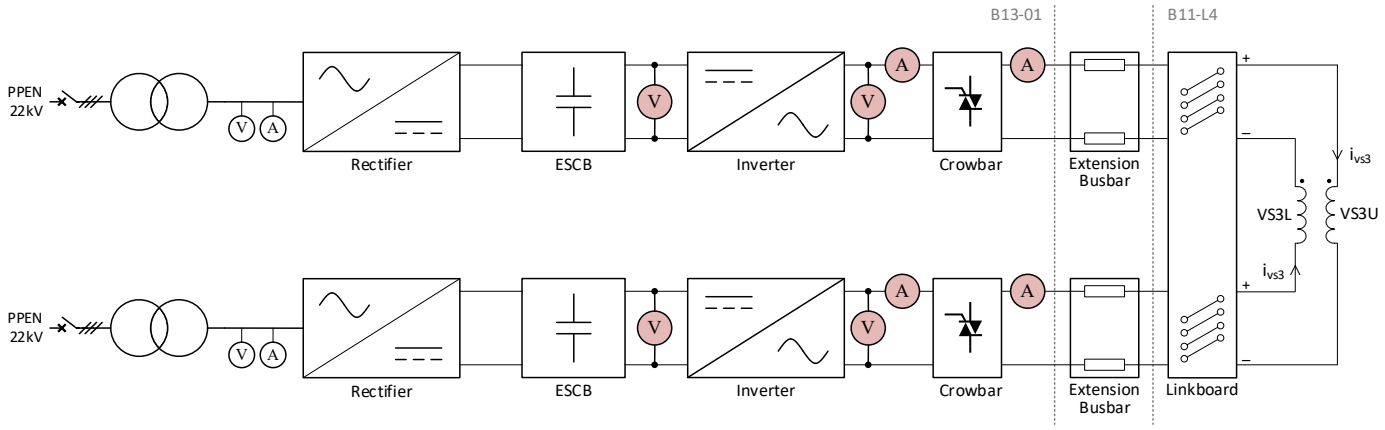

Figure 7-2: VS3 Power Supply architecture with location of measurements relevant to PCS

[4741-005i202-R] The VS3 Power Supply measurements shall comply with the performance requirements listed in Table 7-3.

[I] *Control measurements* are those considered relevant for the real-time control of the vertical stabilization of the plasma, including closed-loop control at PCS. *Monitoring measurements* are those related to the operation of the power supply system and are provided to PCS for estimation of the power supply status. The performance requirements on *Monitoring measurements* are considered as absolute minimum; the actual performance may be better depending on the detailed design of the power supply.

[I] The accuracy specification considers all mechanisms contributing to measurement uncertainty that cannot be compensated or calibrated for, including but not limited to: nonlinearity error, gain error drift and offset error drift. Static gain and offset errors are assumed to be compensated/calibrated for and are not included in the stated accuracy.

[I] The data rate specifies how frequently data is provided to PCS, it does not necessarily correspond to the sampling rate, which may be considerably higher. The currently defined acquisition rate allows for limited anti-aliasing filtering.

Table 7-3: VS3 Power Supply data acquisition requirements

	Control measurements	**Monitoring measurements**
Signals	- *VS-coil current* - *PS output voltage*	- *PS output current* - *PS DC link voltage*
Range	VS coil current: 0…±120 kA PS output voltage: 0…±3 kV	As per PS needs
Accuracy	≤ 0.5% of FSR (current) < 1% of FSR (voltage)	≤ 5% of FSR
Precision	DR ≥ 80 dB SNR ≥ 60 dBFS	DR ≥ 50 dB SNR ≥ 50 dBFS
Bandwidth (-3dB)	Current: DC … ≥ 0.5 kHz [1)] Voltage: DC … ≥ 1 kHz	DC … ≥ 100 Hz
Data rate	Current: ≥ 4 kHz Voltage: 10 kHz	1 kHz
Delay	≤ 1 ms	≤ 10 ms

Note 1: increase of bandwidth may be possible when requirements for anti-aliasing are reduced.

7.3 Status monitoring and reporting

This section defines the requirements in relation to status reporting relevant to PCS.

[4741-005i301-R] The VS3 Power Supply shall report to PCS its operational status with an update rate of at least 100 Hz.

[I] The present definitions for status reporting are conceptual; these will be updated during preliminary and final design stage.

[I] The operational status of the VS3 Power Supply System typically comprises the Operating State (Table 7-4) and specific Status Flags (Table 7-5).

Table 7-4: preliminary operating states of VS3-PS system. Only most relevant substates have been listed [RD7]

State	Description
OFF	VS3-PS is disconnected from MV grid. Most LV equipment is powered off, although I&C systems may remain powered-on depending on the level of shutdown required.
	OFF: Fault VS3-PS is no longer operational due to the occurrence of a severe fault, e.g. by: - Transient Over-current protection - Transient Over-voltage protection - Over-temperature protection, including busbar - Detection of isolated circuit parts: blown fuses - Detection of earth faults - Communication time-outs - Etc.
NON-ACTIVE	VS3-PS is not active; all I&C and auxiliary systems are initialized; the DC Link is de-energized. This mode is typically used in between plasma operations with a long period of inactivity, or when the VS3-PS is not required during physics experiments.
OPERATION	VS3-PS is ready for operation or operational; The DC Link may be energized, and the output of the power supply may be progressively established throughout the sub-states. Operational limitations may apply as signalled by the status flags listed below.
	OPERATION: Tripped VS3-PS DC Link remains energized, yet the output stage is disabled following the detection an operating condition outside of the programmed or design limits. A manual control action is required to return back to the OPERATION:Ready state. Typical conditions triggering the tripped state: - Over-current protection - Over-voltage protection When tripped, the inverter output is disabled. The inverter semiconductor switches no longer receive switching signals, whereas the anti-parallel diodes remain in place. The disabled inverter will act like an open circuit, as long as the coil circuit voltage remains below the DC Link voltage. Nevertheless, a current

	can develop in the coil circuit when the (induced) voltage exceeds the DC Link voltage.
OUT OF SERVICE	VS3-PS is out-of-service when a compulsory shutdown is required, or when a fatal fault has occurred that requires the permanent shutdown until the necessary maintenance or repairs have been performed.

Table 7-5: preliminary definition of Status Flags reported by VS3-PS

Flags	**Description**
ReadyForPulse	VS3-PS is ready to provide a full-performance VDE pulse if requested; refer to [4741-005i302-R]
Degraded	Operation with only 1 out of 2 power converters, i.e. only half the output voltage. Typically resulting from overriding a fault/unavailability of one of the power converters. Only in consultation with operation responsible officer of VS3-PS.
DLC	Power supply circuit is configured for Dummy Load operation, prohibiting energy being provided to VS coil circuit.
OOR	Power supply output is Out-of-Regulation, i.e. the requested voltage in CV mode or requested current in CC mode cannot be achieved; refer to [4741-005i303-R]

[4741-005i302-R] The VS3 Power Supply shall continuously monitor and communicate to PCS its status with respect to the capability of providing a full-performance VDE current pulse.

[I] To be capable of proving a full-performance VDE pulse, as a minimum, the following conditions need to be fulfilled:

- to be in the appropriate Operating State
- to have sufficient thermal margin remaining *
- to have the DC Link voltage at the nominal voltage
- to have ESCB estimated state-of-health above 95%

[I] * The method of determining the operational/thermal capacity is defined by the VS3-PS design and may involve measuring the temperature of critical components but could equally be based on synthetic methods such as considering the history of output current (e.g. pulse counting, I^2*t integral, etc).

[I] Irrespective whether the VS3-PS indicates to be ready for a full pulse or not, PCS may at any time provide setpoints for starting a new VDE pulse. The internal protections of the power supply will ultimately limit and/or abort the pulse, for instance when thermal limits are exceeded, when the DC Link voltage drops below the minimum value, etc. This may result in a tripped (and thus shutdown) power supply.

[4741-005i303-R] The VS3 Power Supply shall communicate to PCS any change in performance level, for instance due to component failures, thermal issues or loss of services such as cooling water, for the purpose of adapting the control to reduced performance of the system or to anticipate failure. The extent to which the Power Supply can provide such information will be detailed while the maturity of the power supply design progresses.

[4741-005i304-R] The VS3 Power Supply shall continuously monitor and report to PCS the output regulation status.

[I] The Out-of-Regulation status is signalled when the power supply is not able to produce the requested voltage or current at the output:

In Controlled Voltage (CV) mode, this may be caused by:

- The voltage setpoint exceeds the OVL value*
- The current required to produce the requested voltage setpoint (static) or the requested voltage waveform slew-rate (dynamic) exceeds the OCL value*

In Controlled Current (CC) mode, this may be caused by:

- The current setpoint exceeds the OCL value*
- The voltage required to produce the requested current setpoint (static) or the requested current waveform slew-rate (dynamic) exceeds the OVL value*

* the OVL/OCL value refers to the most restrictive limit applied: the intrinsic (design ratings), the programmed (user) or the (dynamic) limit applied for thermal protection

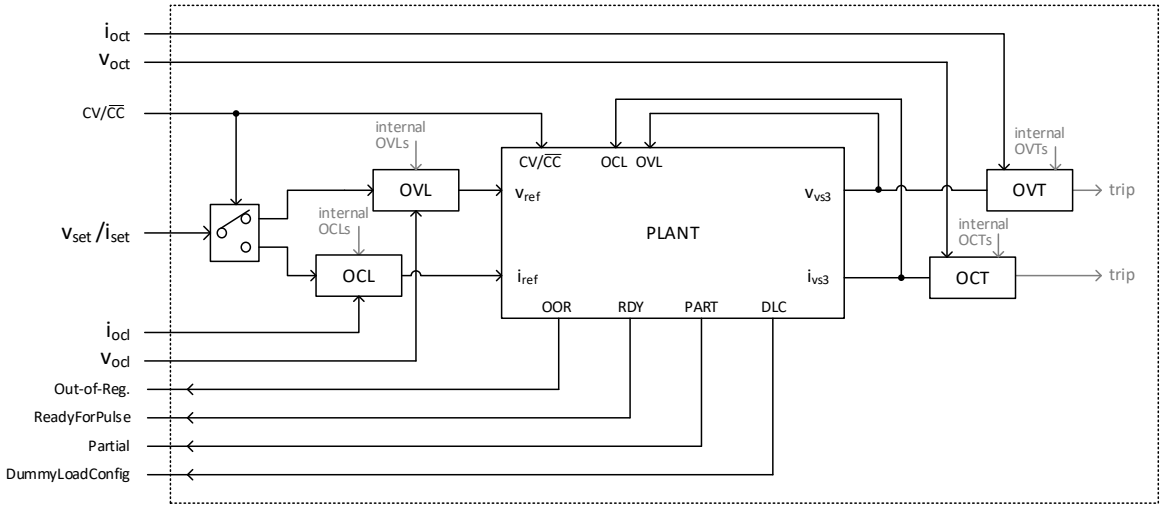

Figure 7-3: preliminary definition of main interface signals between PCS and VS3-PS.

7.4 Control signals from PCS to VS3-PS

[4741-005i401-R] The VS3 Power Supply shall accept two setpoint-related signals from PCS, at a continuous and synchronous rate of 1 kHz: (1) the setpoint value and (2) the requested operating mode, being closed-loop voltage control or closed-loop current control. The transition

between the operating modes shall be immediate and seamlessly within the limits of closed-loop control.

[I] The default operating mode is closed-loop current control, implemented at PCS side, for which the VS3 Power Supply receives voltage setpoints from PCS and provides coil current measurements to PCS.

[I] A dedicated output-on control signal is not foreseen; the power supply is sequenced into the Operation state and the output may simply be controlled by the voltage and current setpoints, e.g. in equivalent-off state (open-circuit) by maintaining the current setpoint at zero.

[4741-005i402-R] PCS's control strategy shall consider the maximum energy available for a VDE pulse and adapt the setpoint values such that the ESCB voltage never drops below the defined minimum DC Link voltage, e.g. 50% of the rated DC voltage.

[I] The VS3 Power Supply will actively limit the output voltage in order to maintain the DC link voltage strictly above the minimum DC voltage, such to avoid excessive (harmonic) currents at the AC-side.

[I] The available energy at 50% of the nominal DC Link voltage is theoretically equal to 75% of the rated energy stored at 100% of the nominal DC link voltage.

[I] The definitive value of the minimum voltage will be defined at FDR stage.

[4741-005i403-R] The VS3 Power Supply shall allow write access to predefined operational parameters, e.g. for monitoring and/or setting parameters in relation to output limiting, tripping and over-voltage/over-current protection.

7.5 General control requirements

[4741-005i501-R] The VS3 Power Supply shall comprise a time-out mechanism (e.g. watchdog) that resets the power supply output voltage and current setpoints to zero in case no new setpoints have been provided by PCS for a configurable interval, in all Operation states.

[I] The continuous transmission of setpoints may be used for this purpose

[4741-005i502-R] PBS 41 shall provide design documentation containing an exhaustive description of all protection mechanisms incorporated in the VS3 Power Supply, including all associated protection threshold levels, in order to allow PCS to perform real-time state estimation of the protections (e.g. I^2*t integral value) for limiting/tripping avoidance purposes.

8 Division of Responsibilities

PBS 41 shall ensure that the design, control and operation of VS3-PS is compliant with the interface requirements set forth in this interface sheet.

PBS 47 shall design the PCS and operate the VS3-PS through PCS in accordance with the interface requirements set out in this interface sheet.

8.1 Responsibilities regarding VS3 coil circuit

The PCS shall operate in a way to maintain the current reference and voltage reference within the operational limits of the coils by providing dedicated control strategies, but it has no responsibilities in preventing these limits from being exceeded due to the coupling between the VS coils, the plasma and the vacuum vessel.

The VS3-PS has no responsibility in ensuring that the thermal limits of the VS coils are not exceeded. Indeed, VS3-PS has no knowledge of the momentary thermal conditions of the VS coil turns and no knowledge of other heating, e.g. nuclear heating, to the coil, and being a pulsed power system, specific combinations of pulses may potentially lead to exceeding the thermal limits. PBS 15.IV has the responsibility of monitoring the temperature of the IVCs and raising the warning, alarms and interlock events when the limits are approaching or exceeded. The activity is linked with the Central Interlock System (CIS).

The VS3-PS shall allow external interlocks transmitted over CIS to immediately stop the power supply operation. Upon shutdown, the magnetic energy in the VS3 coil circuit is either dissipated in the coil circuit through activation of the crowbar or discharged in the DC Link in the absence thereof. Irrespective of the method used, the VS3-PS shall ensure that the load circuit is de-energized in a controlled and safe manner.

The VS3-PS shall ensure that during normal operation the rated operating voltage and current levels of the power supply are not exceeded, for instance through the implementation of over-current and over-voltage limiting and tripping.

The VS3-PS shall equally monitor the earth current in the VS3 coil circuit and ensure that the appropriate action is taken upon detection of the first earth fault, such as the immediate shutdown of the power supply and coil circuit.

The VS3-PS is responsible for ensuring that the thermal limits of the VS3 busbar system, comprising the Extension Busbars, the Linkboard and IVC busbars, are not exceeded. For that purpose, the cooling water return temperature and flow will be monitored and the appropriate actions will be taken by the VS3-PS local Plant Control System.

8.1.1 VDEs & Plasma Disruptions

The impact on the VS coils of transient plasma events combined with control pulses provided by VS3-PS has been assessed in [RD5]. The maximum current magnitude in the VS3 coil circuit has been calculated at 95.4 kA for 6-turn operation (with 80kA control pulse) and 86 kA for 8-turn operation (with 60kA control pulse). The VS coil and feeder have adopted the peak current for 8-turn operation as design load case [RD6].

The responsibilities of PCS and VS3-PS in this regard are as follows.

During any transient event, the VS3-PS will try to regulate and maintain the output current around the setpoint as long as sufficient voltage is available and as far as the control bandwidth allows. Hence an inverse voltage will be generated to counteract the induced voltage.

Beyond the dynamic capabilities and ratings of the power supply, an excess current will develop in the coil circuit until the over-current protection triggers the crowbar to protect the power supply. At this stage, the VS3 coil circuit is short-circuited, hence the power supply has no control over the coil current.

Hence, the responsibility of the VS3-PS in regard of plasma transients is limited to contributing to the avoidance of significant over-currents in the VS3 coil circuit, to the extent of its capabilities. PCS has no specific responsibilities in this regard.

8.1.2 Over-voltage protection

The VS3-PS shall ensure that the voltage at the input terminals of the VS3 coil circuit does not exceed the rated value (2.4 kV). Nevertheless, the VS3-PS has no responsibility in protecting the VS3 coil circuit against (induced) over-voltages while it is in non-operational states, neither does VS3-PS have responsibilities in relation to disconnected VS-coil turns.

9 Staged Approach

The configuration of the VS3 Power Supply (41.V3) and the Plasma Control System (47) in each of the stages of the Staged Approach is described in [AD7].